REMARKS

Present Status of the Application

Claims 1-7 remain pending of which claim 1 have been amended to more explicitly describe the claimed invention. It is believed that no new matter adds by way of amendment to claims or otherwise to the application.

In the Office Action, claims 1-4 were rejected under 35 U.S.C. 102(b) or 102(e) as being anticipated by Chen et al. (US 2003/0116534); claims 1 and 6 were rejected under 35 U.S.C. 102(b) as being anticipated by Jang et al. (US 2002/0045332); claim 5 was rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 2003/0116534) or over Jang et al. (US 2002/0045332); and claim 7 was rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 2003/0116534) or Jang et al. (US 2002/0045332), each one individually in view of Yates (US 2004/0157448).

Discussion of Office Action Rejections

1. The Office Action rejected claims 1-4 under 35 U.S.C. 102(a) or 102(e) as being anticipated by Chen et al. (US 2003/0116534). Applicants respectfully traverse the rejections for at least the reasons set forth below.

Independent claim 1 recites the features as follows:

1. A cleaning method used in an interconnect process, comprising the steps of:

providing a substrate having a conductive layer and a dielectric layer formed thereon, wherein the conductive layer is formed over the substrate and the dielectric layer is formed over the conductive layer;

removing a portion of the dielectric layer to form an opening in the dielectric layer to expose a portion of the conductive layer; and

cleaning the opening ***in the dielectric layer*** using a mixture containing sulfuric acid and hydrogen peroxide in water.

(emphasis added).

Claims 2-3 also recite the similar features.

In US 2003/0116534, Chen et al. disclosed a method of metal etching post cleaning. The disclosure discussed by Chen et al. is illustrated as below.

[0017] In FIG. 3, **a first ashing is performed using oxygen as a chemical reaction gas to remove the patterned resist layers 24a on the patterned aluminum layers 22a**.

[0018] In FIG. 4, **after the resist layers 24a are removed,** the surface of aluminum layers 22a exposed retains polymer residue 25 created during the first ashing and accumulates charges created during aluminum layer 22 etching. **Accordingly, in this embodiment, a second ashing is performed using ozone to release the charges 23 accumulated on the surface of the patterned aluminum layers 22a.** Here, the second ashing temperature is 200 degree about.300 degree. Moreover, the second ashing time is 30 sec.about.180 sec, and 120 sec is preferred. Hence, aluminum oxide (Al_2O_3) thin layer (not shown) is formed on the surface of the patterned aluminum layers 22a by a reaction between aluminum and ozone at high temperature. The object of this is described later.

[0019] In FIG. 5, **the mixtures of sulfuric peroxide (i.e. sulfuric acid and hydrogen peroxide) and de-ionized water (DIW) are used as a cleaning agent to cleaning the aluminum layers 22a, thereby removing polymer residue 25 as mentioned above.** In this embodiment, the molar concentration of sulfuric acid contained in the sulfuric peroxide is 0.07M.about.0.4M, and 0.13M is preferred. Moreover, the molar concentration of hydrogen peroxide contained in the sulfuric peroxide is 0.8M.about.1.5M, and 1.18M is preferred. In addition, the temperature of sulfuric peroxide during post cleaning is 25 degree C about.50 degree C, and 34 degree C is preferred. Hence, it is effective to remove polymer residue 25.

After studying paragraph [0017]-[0019], Applicant assert that the method of meral etching post cleaning disclosed by Chen et al. is not equivalent to claim 1. As shown in FIG. 5 and the related description, **the mixtures of sulfuric peroxide (i.e. sulfuric acid and hydrogen peroxide) and de-ionized water (DIW) are used as a cleaning agent to cleaning the aluminum layers 22a, thereby removing polymer residue 25 as mentioned above.** Still referring to FIG. 5 and the related description, after performing the second ashing, the resist layers 24a disclosed by Chen et al. have been removed completely and polymer residue 25 is retained on the surface of the patterned aluminum layers 22a. Specifically, the mixtures of sulfuric peroxide (i.e. sulfuric acid and hydrogen peroxide) and de-ionized water (DIW) disclosed by Chen et al. are "NOT" used to clean the opening in the resist layers 24a. In other words, the subjects to be cleaned in the citation and the present invention are absolutely different from each other. Accordingly, the disclosure of Chen et al. is not read on claim 1.

In comparison with the resist layers 24a disclosed by Chen et al., the dielectric layer recited in claim 1 is an inter-layer of interconnection and would not be removed completely. The resist layers 24a disclosed by Chen et al. are used as a mask for defining the pattern of the patterned aluminum layers 22a and the resist layers 24a are not a portion of interconnection. Therefore, claim 1 is distinguished from prior art (US 2003/0116534) and is in proper condition for allowance.

If independent claim 1 is allowable over the prior art of record, then its dependent claims 2-4 are allowable as a matter of law, because these dependent claims contain all

features of their respective independent claim 1. In re Fine, 837 F.2d 1071 (Fed. Cir. 1988).

2. The Office Action rejected claims 1 and 6 under 35 U.S.C. 102(b) as being anticipated by Jang et al. (US 2002/0045332). Applicants respectfully traverse the rejections for at least the reasons set forth below.

In US 2002/0045332, Jang et al. disclosed a method of fabricating a semiconductor device using a damascene metal gate. The disclosure discussed by Jang et al. is illustrated as below.

[0040] Referring to FIG. 9, **the exposed damascene gate electrode 33 is etched in part by known either a dry etch or wet etch process so as to form a trench 37** having a thickness of between 500 to 1000 .ANG. at an upper part of the damascene gate electrode 33a. In this case, the etched portion of the damascene gate electrode 33 is removed by a recessed-etch process.

[0042] The selective growth of the aluminum layer 38 is explained in detail as follows. First, a cleaning process is carried out before growing so as to make the Al grow selectively. The cleaning process is carried out on the exposed damascene gate electrode 33a using H_2SO_4 and H_2O_2, thereby enabling the removal of organic impurities.

[0045] Referring to FIG. 11, **following the growth of the aluminum layer 38, an insulating layer 39 is formed in the trench 37 over the upper part of the damascene gate electrode 33a. For instance, the insulating layer 39 is formed by oxidizing the aluminum layer 38 in the trench 37 into an aluminum oxide layer (Al_2O_3).**

[0049] Referring to FIG. 13, contact holes 42 are formed by selectively etching the insulating interlayer 40 using a photoresist layer 41 as a mask so as to expose the source/drain regions 34. In this case, the contact holes 42 are used to provide a bit line contact and/or a storage electrode contact when the method of fabricating a semiconductor device according to the present invention is applied to a memory device such as a DRAM. Although non-uniformity is generated when the contact holes 42 are formed, the damascene gate electrode 33a is not exposed since the upper part of the damascene gate electrode 33a is covered with the insulating layer 39.

[0054] First, a first cleaning step is carried out before the growing so as to make silicon grow selectively. In this case, the first cleaning step is carried out on the exposed damascene gate electrode 53a using H_2SO_4 and H_2O_2 so as to remove organic impurities. The first cleaning step preferably is processed in a mixture solution having a ratio of

between 30 to 50:1 between H_2SO_4 and H_2O_2 for a period of between 5 to 20 minutes at a process temperature between 60 to 100.degree. C.

After studying paragraph [0040]-[0054], Applicant assert that the method of fabricating a semiconductor device using a damascene metal gate disclosed by Jang et al. is not equivalent to claim 1. As shown in FIG. 9 and the related description (paragraph [0040]), the trench 37 disclosed by Jang et al. is formed by etching the exposed damascene gate electrode 33. In contrary, the opening in the dielectric of the present invention is formed by ***removing a portion of the dielectric layer***. Therefore, the fabricating method disclosed by Chen et al. is not equivalent to claim 1 and in proper condition for allowance.

If independent claim 1 is allowable over the prior art of record, then its dependent claim 6 is allowable as a matter of law, because these dependent claims contain all features of their respective independent claim 1. In re Fine, 837 F.2d 1071 (Fed. Cir. 1988).

3. The Office Action rejected claim 5 under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 2003/0116534) or over Jang et al. (US 2002/0045332). Applicants respectfully traverse the rejections for at least the reasons set forth below.

As described above, the process disclosed in US 2003/0116534 and US 2002/0045332 is quite different from claim 1. Applicant asserts that it is difficult for one skilled artisan to associate claim 1 of the present invention with the process disclosed in US 2003/0116534 and US 2002/0045332. Therefore, claims 1 and 5 are in proper condition for allowance.

4. The Office Action rejected claim 7 under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 2003/0116534) or Jang et al. (US 2002/0045332), each one individually in view of Yates (US 2004/0157448). Applicants respectfully traverse the rejections for at least the reasons set forth below.

As described above, the process disclosed in US 2003/0116534 and US 2002/0045332 is quite different from claim 1. Applicant asserts that it is difficult for one skilled artisan to associate claim 1 of the present invention with the process disclosed in US 2003/0116534 and US 2002/0045332. Even the disclosure of Yates (US 2004/0157448) can be combined with US 2003/0116534 and US 2002/0045332, the result still different from claim 7 of the present invention. Therefore, claim 7 is in proper condition for allowance.

For at least the foregoing reasons, Applicant respectfully submits that claims 1-7 are in proper condition for allowance. Reconsideration is respectfully requested.

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CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1-7 are in proper condition for allowance. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel to arrange for such a conference.

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